


Bitland Confidential

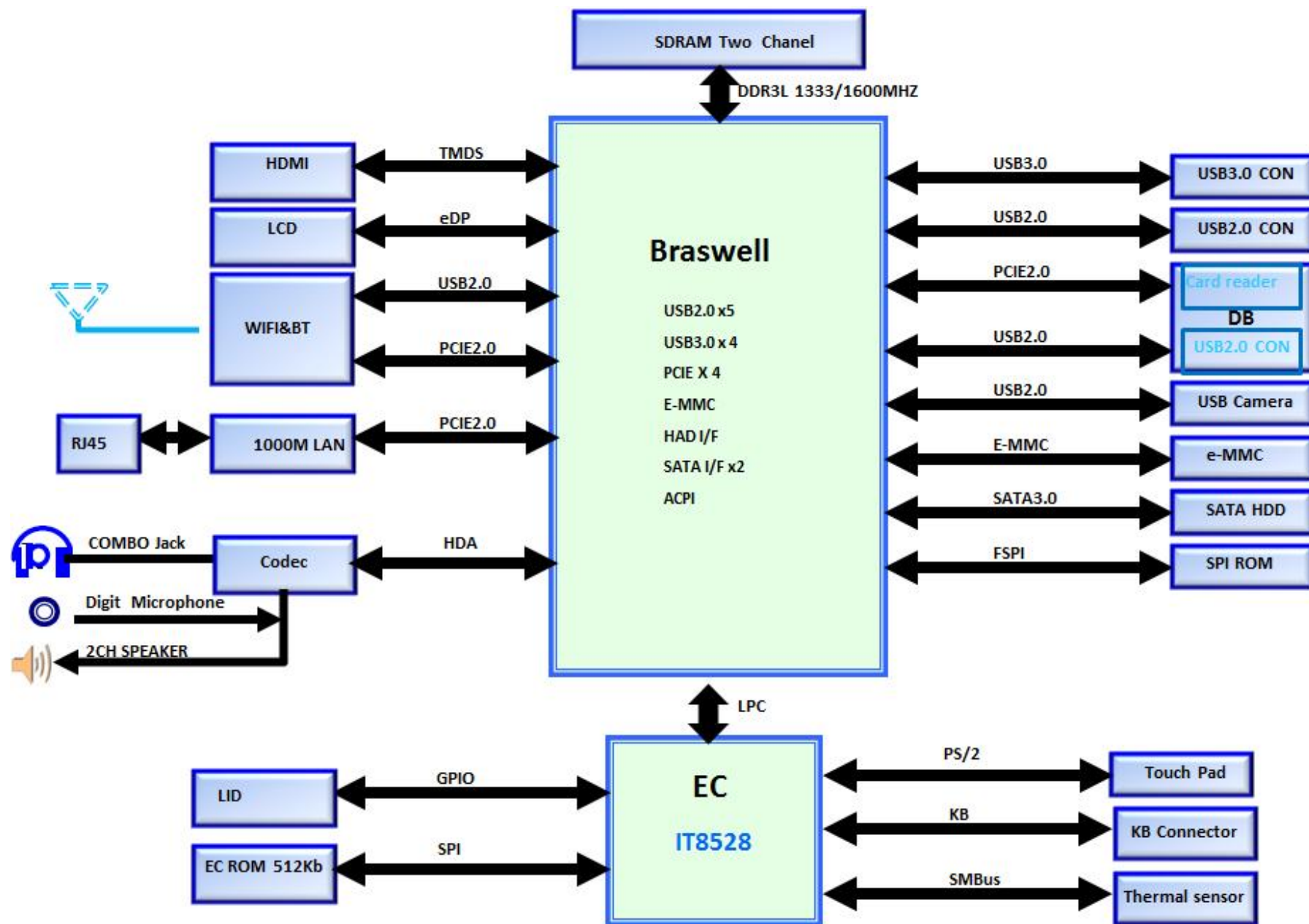
M/B Schematics Document

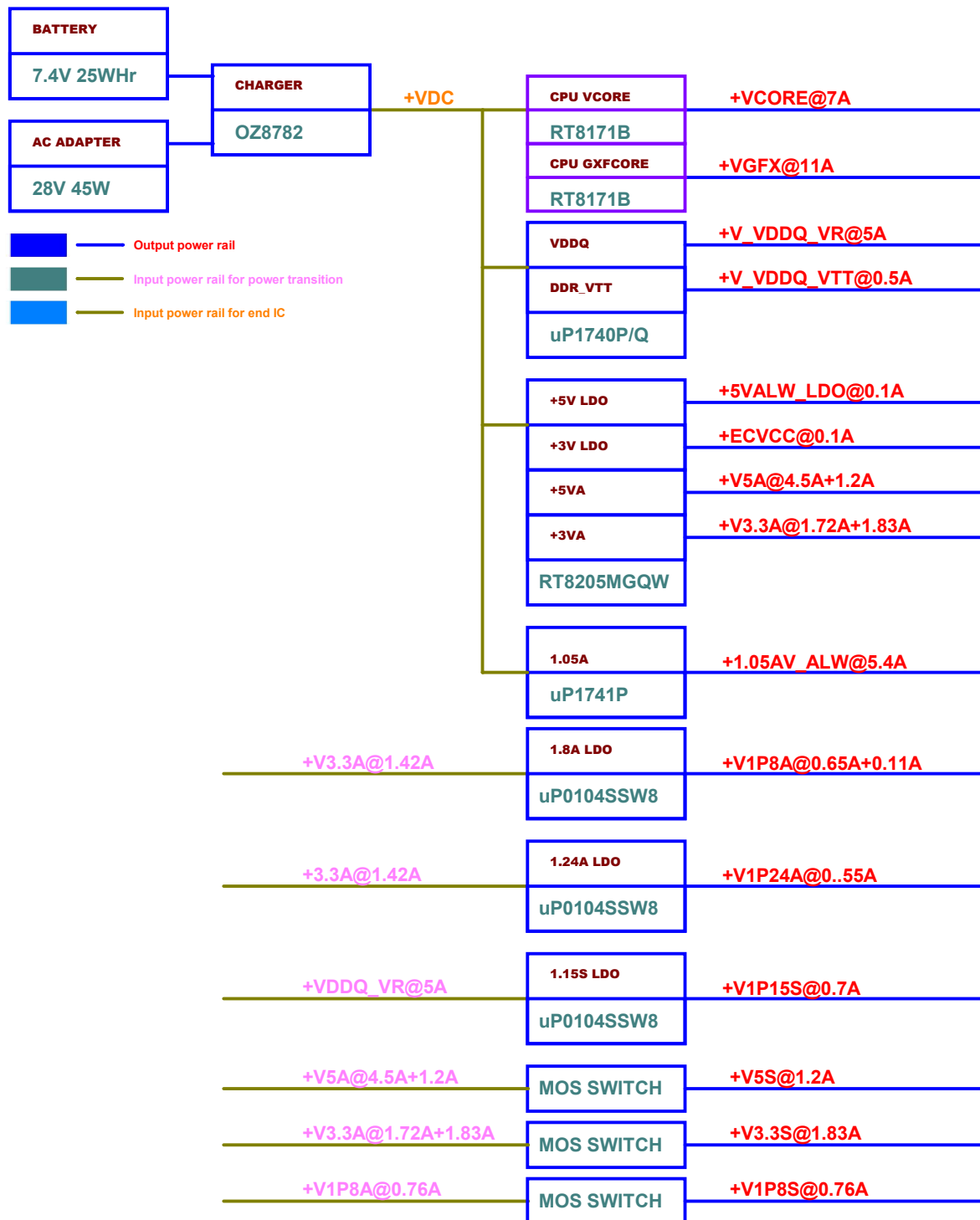
Intel Braswell-M Platform

V1.2

2015-04-15

		Bitland Information Technology Co.,Ltd.	
Page Name Cover Page			
Size A3	Project Name Braswell-M		Rev 1.0
Date: Tuesday, June 09, 2015 Sheet 1 of 52			
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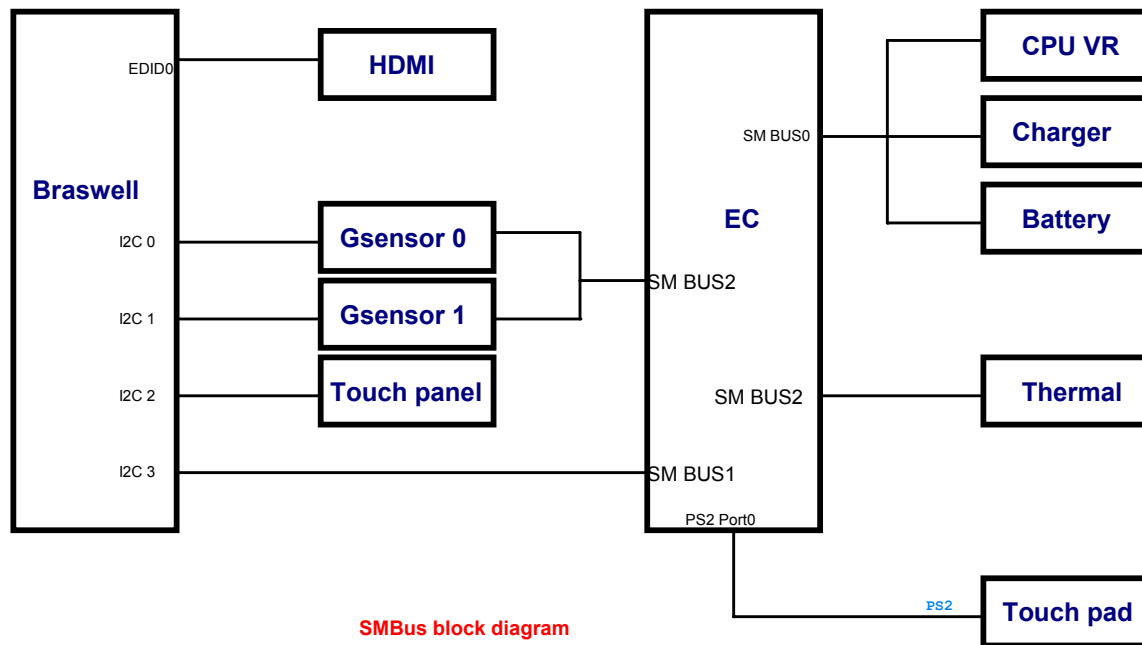




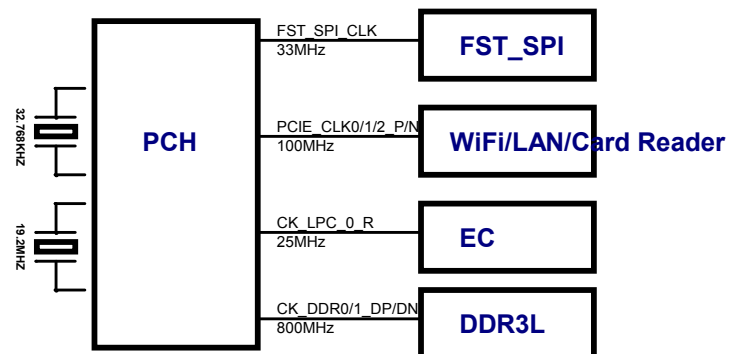
Power States

Power Rail	On S0	On S3	On S4/S5	On G3
VRTC	ON	ON	ON	ON
VCore1/0	ON	OFF	OFF	OFF
VGG	ON	OFF	OFF	OFF
VDDQ_VTT	ON	OFF	OFF	OFF
+V1. 8S	ON	OFF	OFF	OFF
+V3. 3S	ON	OFF	OFF	OFF
+V5S	ON	OFF	OFF	OFF
+V1. 15S	ON	OFF	OFF	OFF
VDDQ_VR	ON	ON	OFF	OFF
+V3. 3A_PRIME	ON	ON	ON	OFF
+V1. 8A	ON	ON	ON	OFF
+V1. 24A	ON	ON	ON	OFF
+V1. 05A	ON	ON	ON	OFF
+V3. 3A	ON	ON	ON	OFF
+V5A	ON	ON	ON	OFF





SMBus block diagram



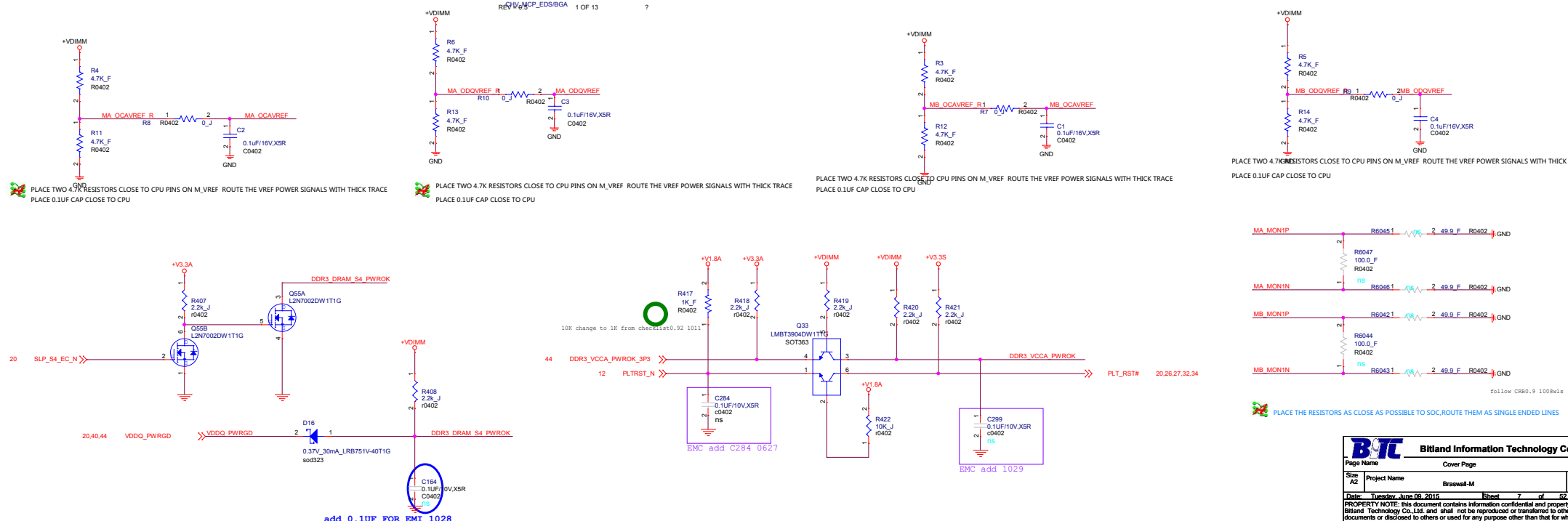
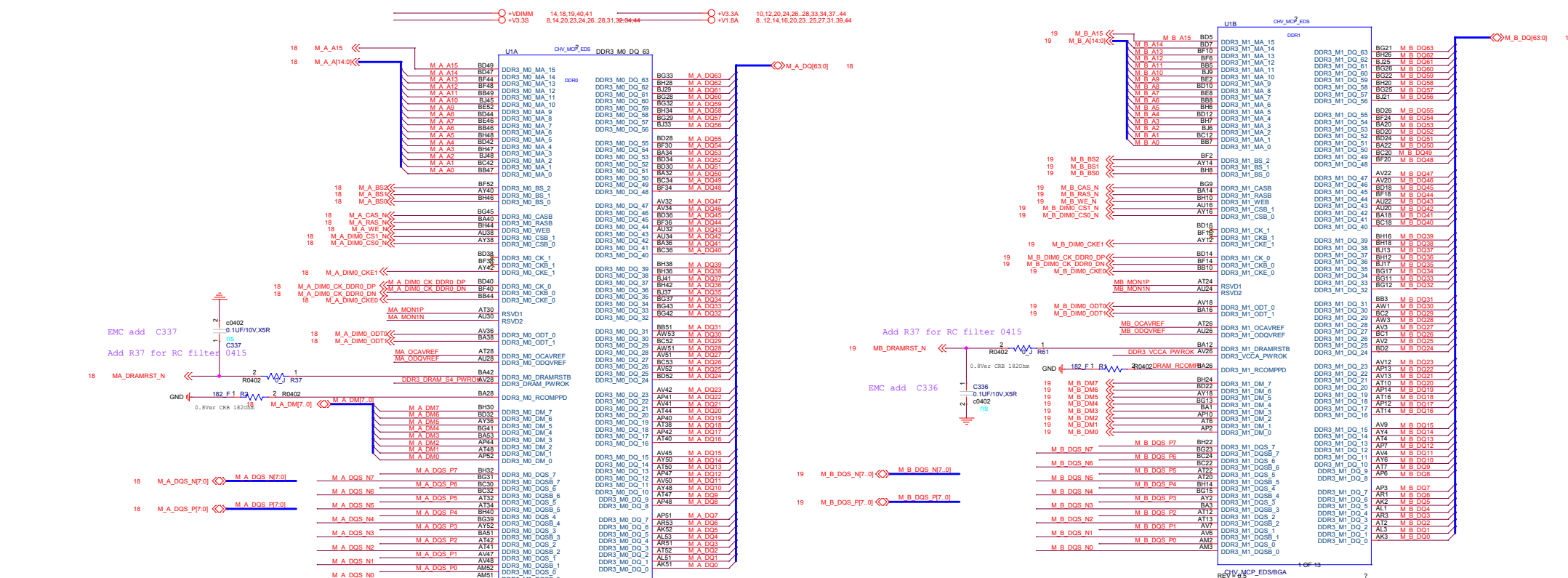
Clock block diagram

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1



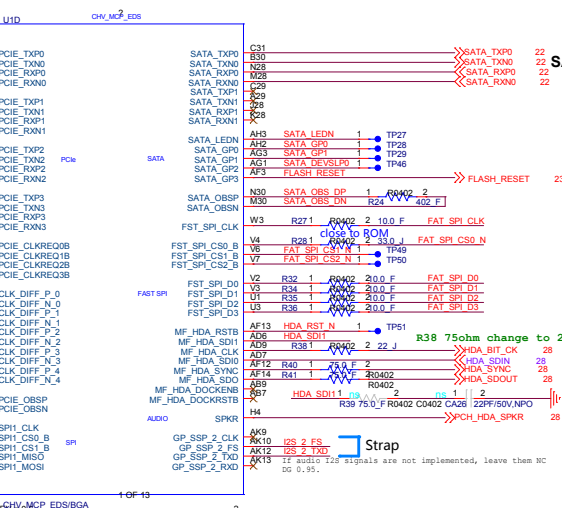
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Size B	Project Name Braswall-M	Rev 1.0	
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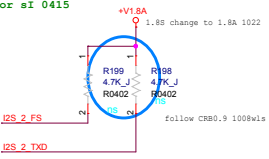


+V1.8A 7,8,10,12,14,16,20,23,25,27,31,39,44

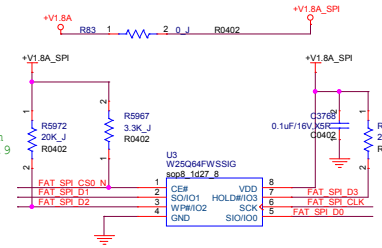
+V1.8S 10,14,20,23,28,31,44

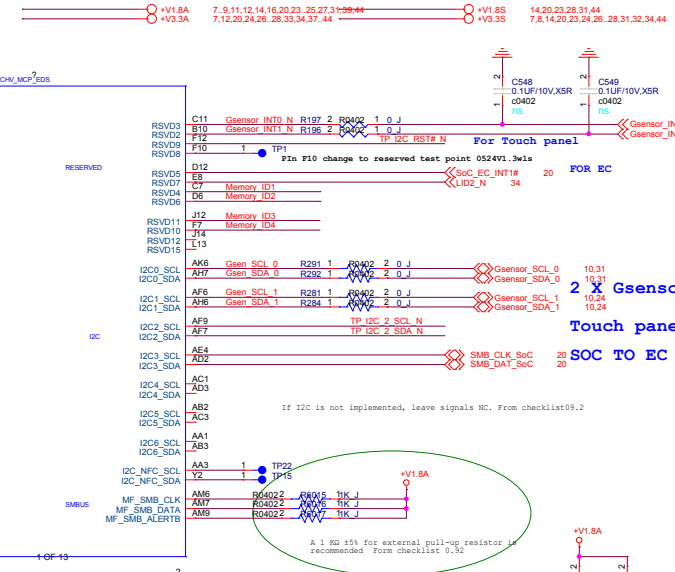
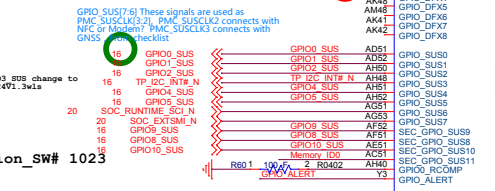
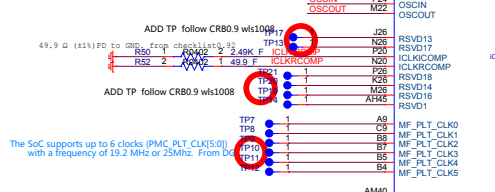
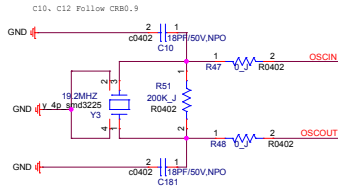


SATA GP[0] is multiplexed with ISB GPIO12.
SATA GP[1] is multiplexed with SPI3 CS[0]
SATA GP[2] is multiplexed with DATA_DEVSLP[0].
SATA GP[3] is multiplexed with DATA_DEVSLP[1].
NMI1_RESET_9, SPI1_CS[4] from R250.52



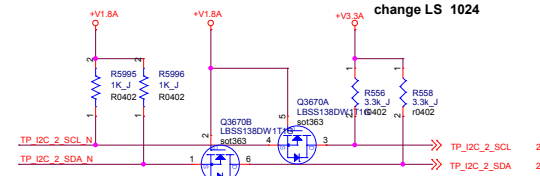
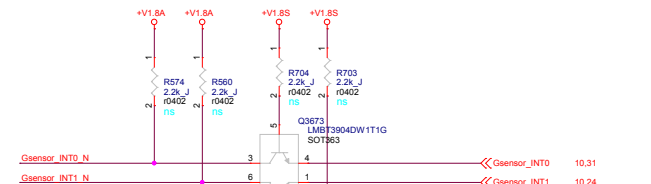
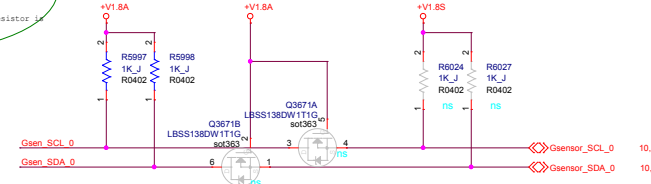
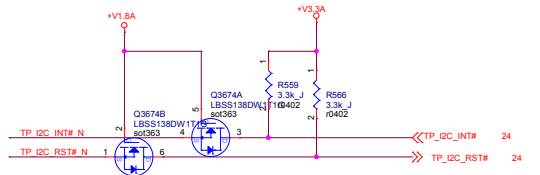
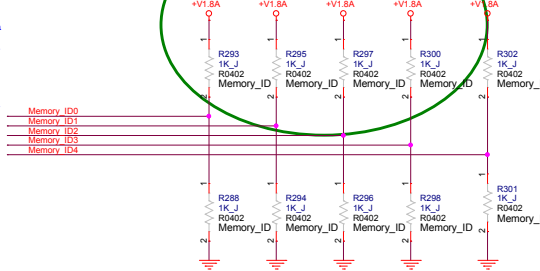
CS need 100 KΩ PU to +V1P8A_SPI From checklist 0.92 , 3.3K PU from CRB 0.9 D2, D3 PU 20K from CRB0.9



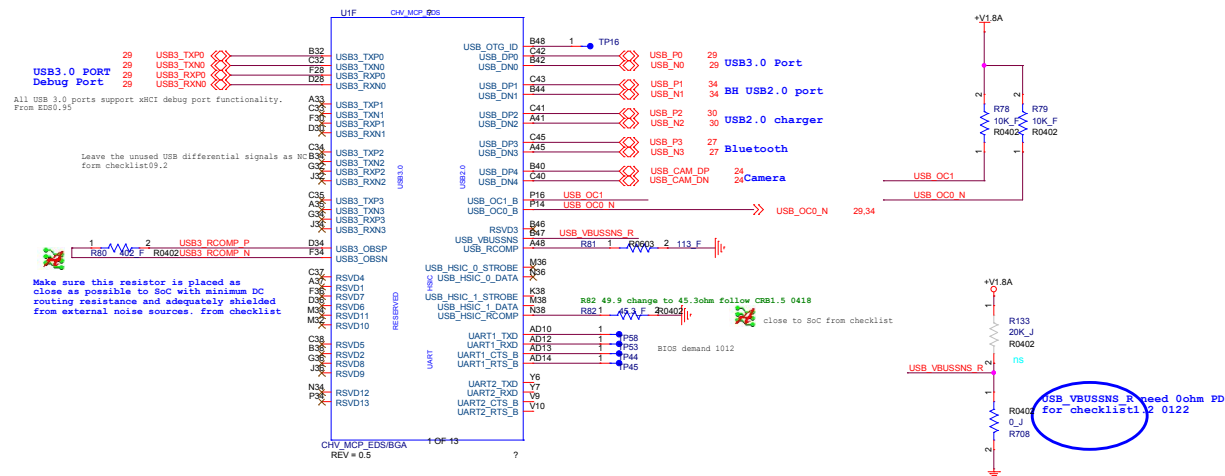


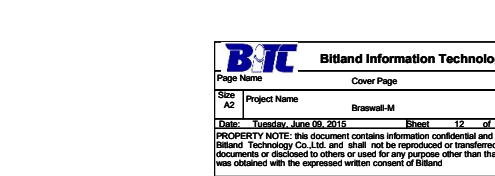
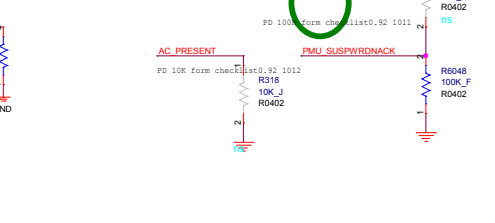
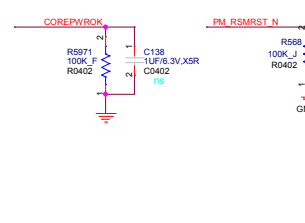
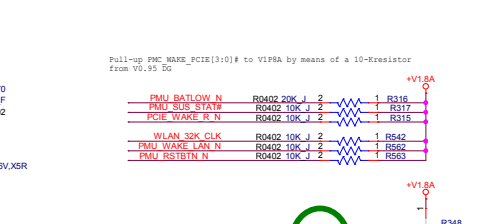
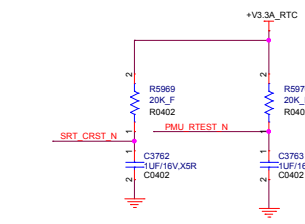
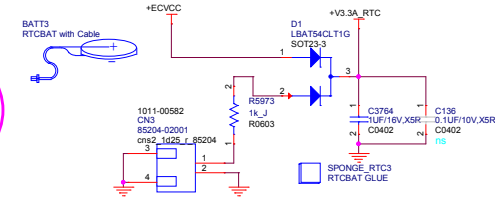
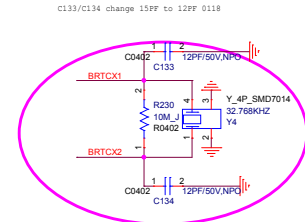
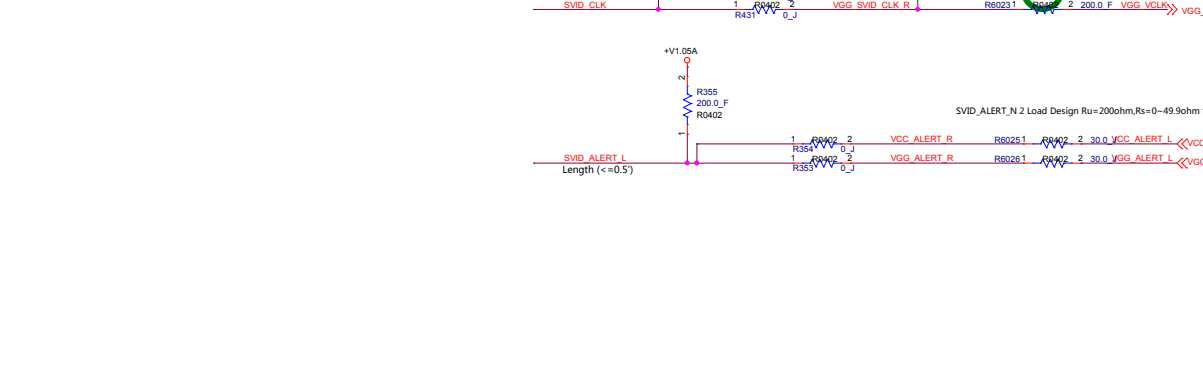
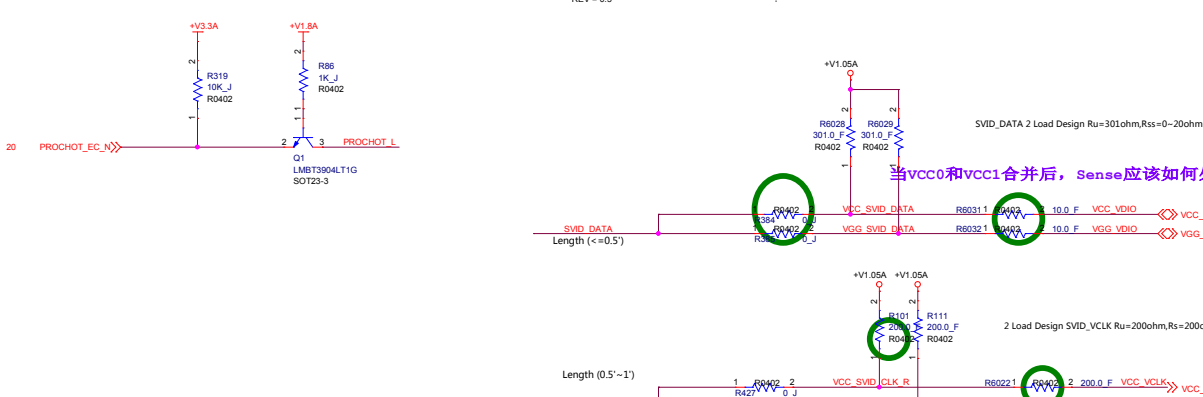
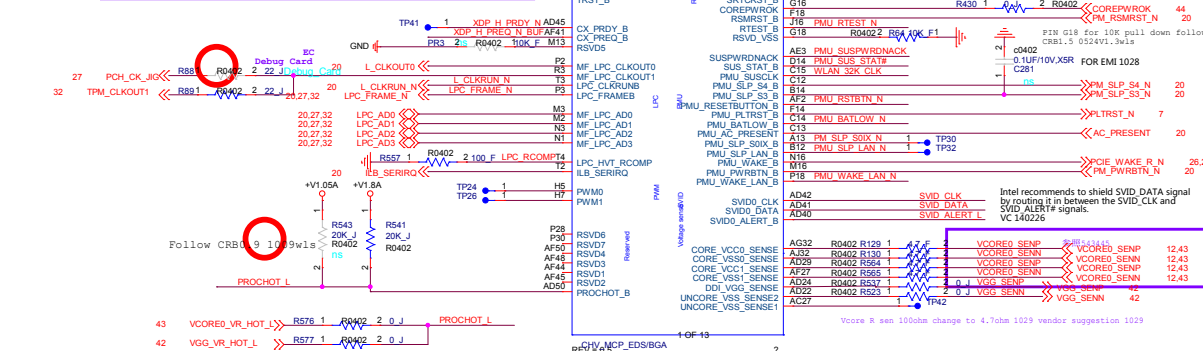
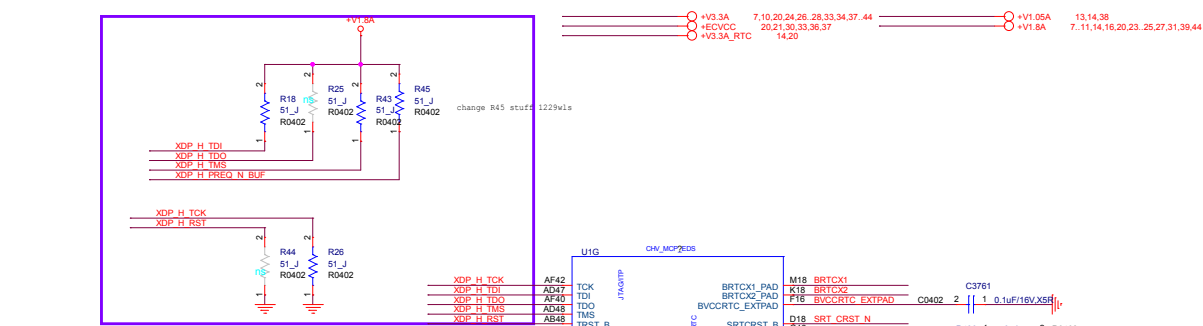
Memory_ID0	Memory_ID2	Memory_ID3	Memory_ID4	SDRAM Configuration
0(R294)	0(R296)	0(R298)	0(R301)	Hynix H5TC4G63AFR-PBA
0(R294)	0(R296)	0(R298)	1(R302)	Hynix H5TC8G63AMR-PBA
0(R294)	0(R296)	1(R300)	0(R301)	Micron MT41K256M16HA-125:B
0(R294)	0(R296)	1(R300)	1(R302)	Micron MT41K512M16TNA-125:B
0(R294)	1(R297)	0(R298)	0(R301)	Elpida EDJ4216EFBG-GN-F
0(R294)	1(R297)	0(R298)	1(R302)	Elpida EDJ416E6MB-GN-F
0(R294)	1(R297)	1(R300)	0(R301)	Samsung K4B4G164Q-HYK0
0(R294)	1(R297)	1(R300)	1(R302)	Samsung K4B6G164Q-MYK0
1(R295)	0(R296)	0(R298)	0(R301)	Hynix H5TC2G63FFR-PBA
1(R295)	0(R296)	0(R298)	1(R302)	Micron MT41K128M16JT-125K
1(R295)	0(R296)	1(R300)	0(R301)	Samsung K4B2G164Q-BYK0

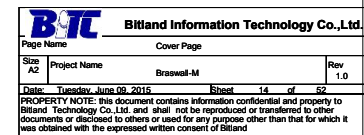
Memory_ID0	Channel Configuration
1(R293)	Single
0(R288)	Double

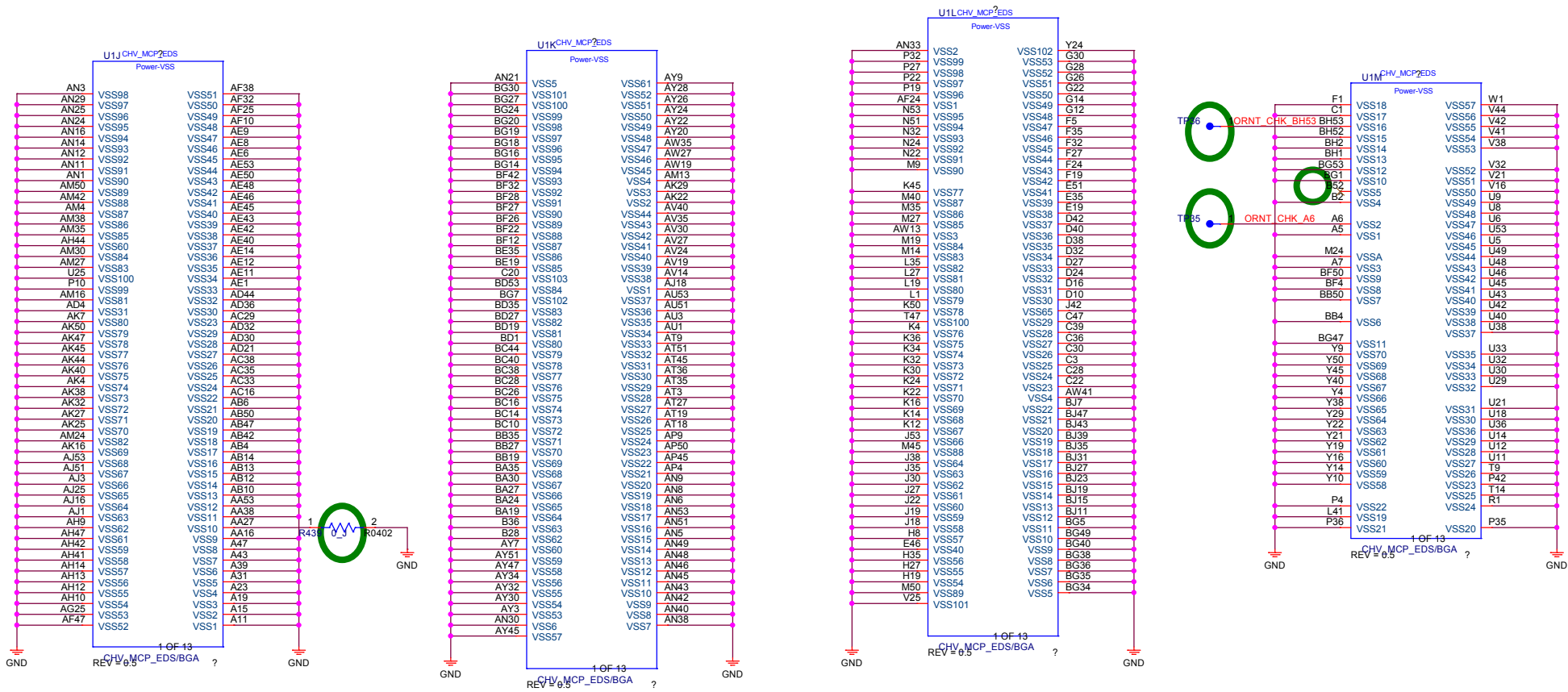


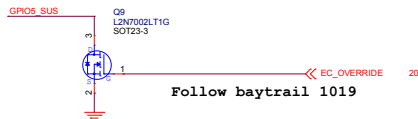
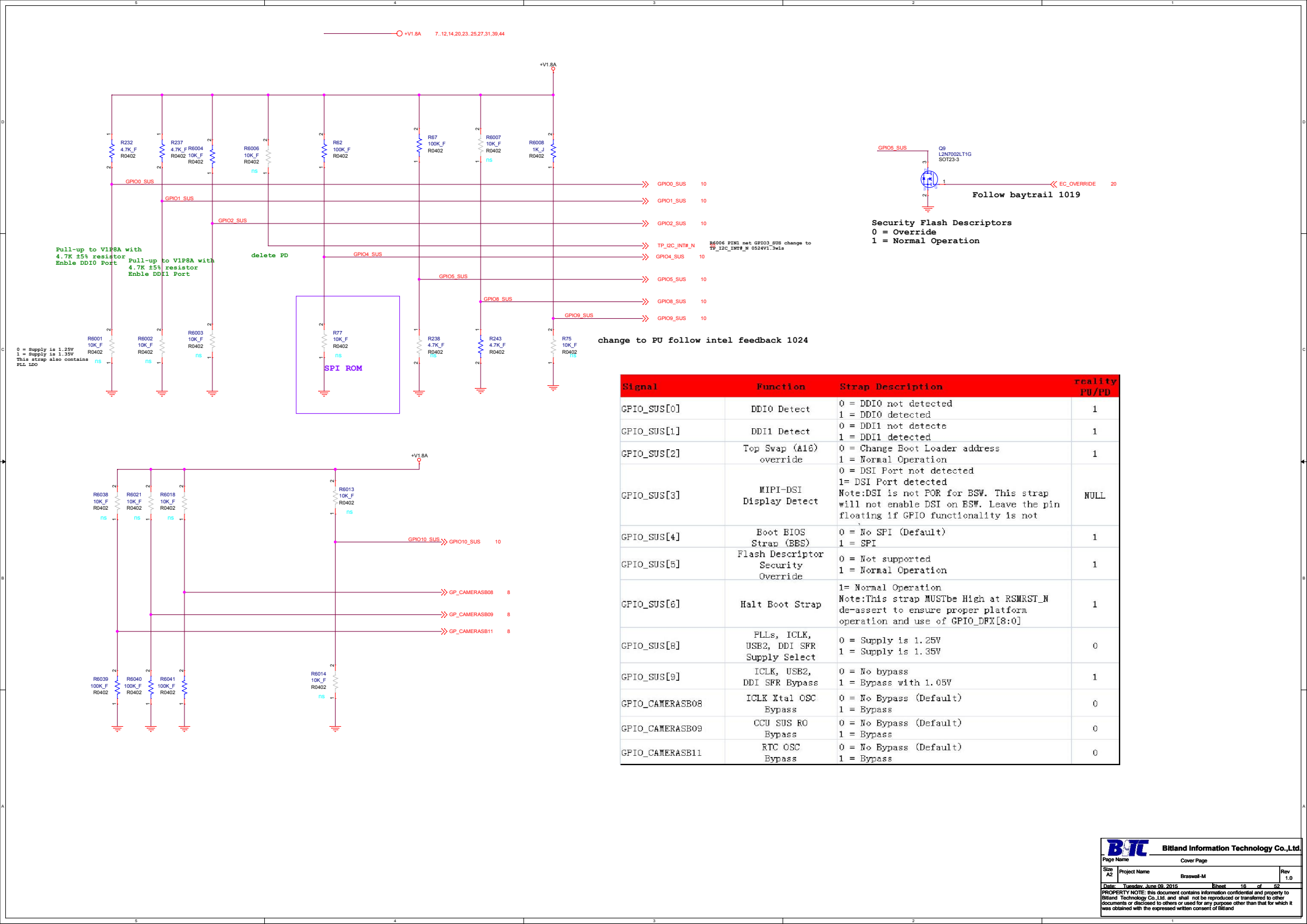
Reserved 3.3K vendor suggestion1210












Security Flash Descriptors
0 = Override
1 = Normal Operation

Signal	Function	Strap Description	reality PU/PD
GPIO_SUS[0]	DDIO Detect	0 = DDIO not detected 1 = DDIO detected	1
GPIO_SUS[1]	DDI1 Detect	0 = DDI1 not detected 1 = DDI1 detected	1
GPIO_SUS[2]	Top Swap (A16) override	0 = Change Boot Loader address 1 = Normal Operation	1
GPIO_SUS[3]	MIPI-DSI Display Detect	0 = DSI Port not detected 1 = DSI Port detected Note:DSI is not POR for BSW. This strap will not enable DSI on BSW. Leave the pin floating if GPIO functionality is not	NULL
GPIO_SUS[4]	Boot BIOS Strap (BBS)	0 = No SPI (Default) 1 = SPI	1
GPIO_SUS[5]	Flash Descriptor Security Override	0 = Not supported 1 = Normal Operation	1
GPIO_SUS[6]	Halt Boot Strap	1= Normal Operation Note:This strap MUSTbe High at RSMRST_N de-assert to ensure proper platform operation and use of GPIO_DFX[8:0]	1
GPIO_SUS[8]	PLLs, ICLK, USB2, DDI SFR Supply Select	0 = Supply is 1.25V 1 = Supply is 1.35V	0
GPIO_SUS[9]	ICLK, USB2, DDI SFR Bypass	0 = No bypass 1 = Bypass with 1.05V	1
GPIO_CAMERASB08	ICLK Ital OSC Bypass	0 = No Bypass (Default) 1 = Bypass	0
GPIO_CAMERASB09	CCU SUS RO Bypass	0 = No Bypass (Default) 1 = Bypass	0
GPIO_CAMERASB11	RTC OSC Bypass	0 = No Bypass (Default) 1 = Bypass	0

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1



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Page Name

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Size

A

Project Name

Braswall-M

Rev

1.0

Date:

Tuesday, June 09, 2015

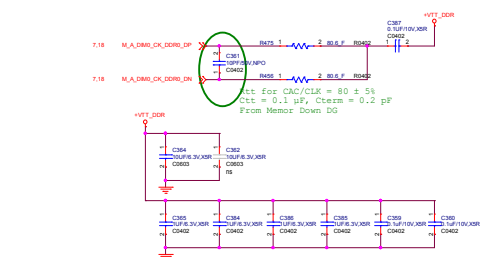
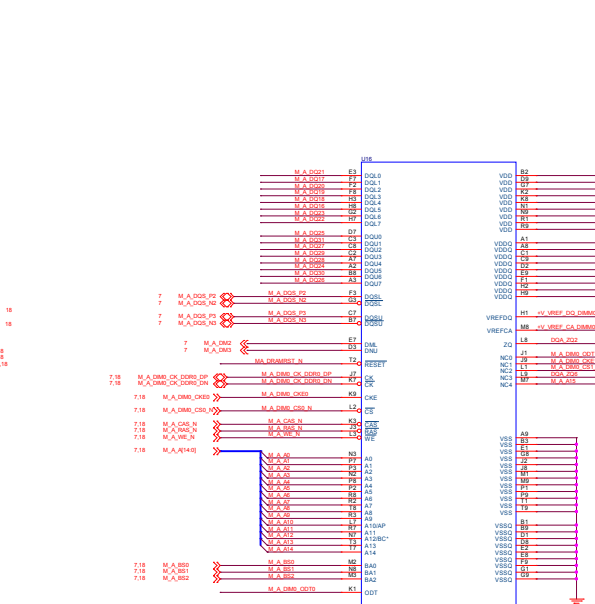
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The figure contains two schematic diagrams of reference voltage blocks.

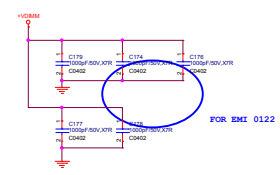
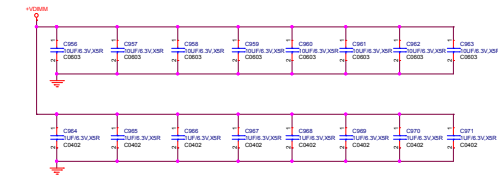
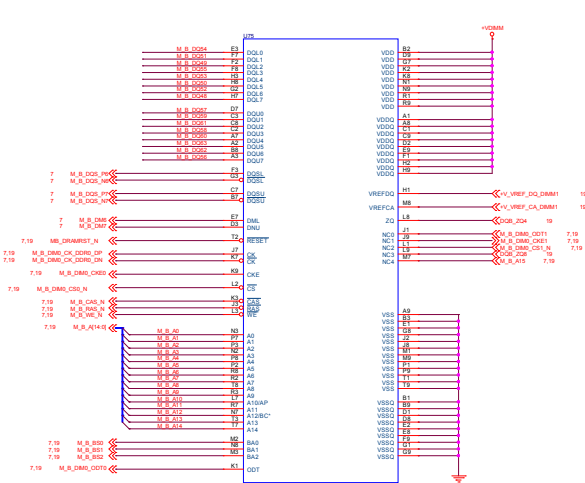
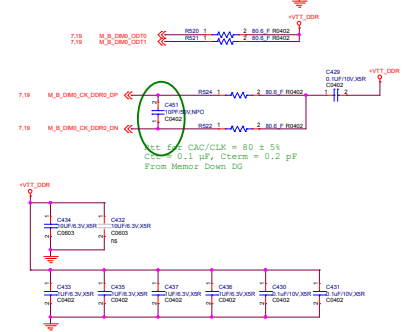
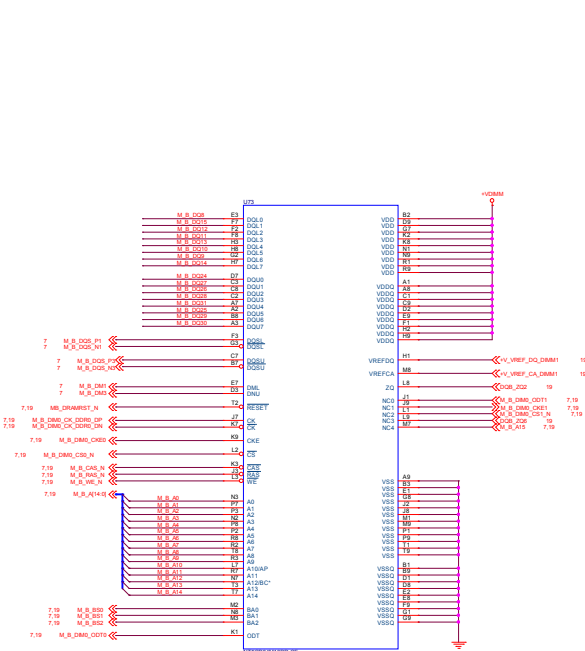
Top Diagram: VREF Block

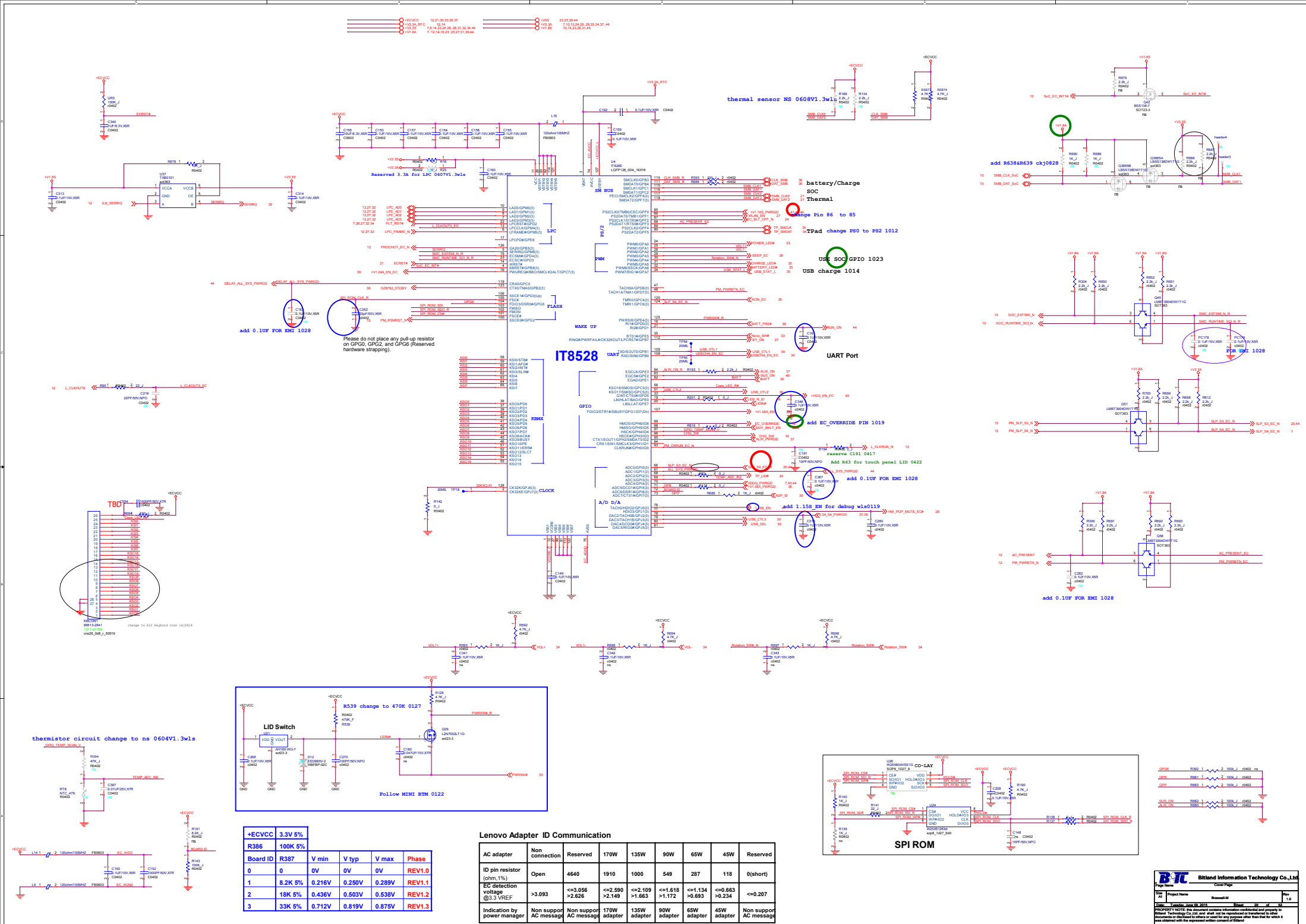
- Inputs:**
 - VREF_P:** Connected to the non-inverting inputs of comparators C350, C351, C352, and C353.
 - VREF_N:** Connected to the inverting inputs of comparators C350, C351, C352, and C353.
- Resistor Network:**
 - A resistor network is connected to the VREF_P input, consisting of a 47K_F resistor in series with a parallel combination of a 100K_F resistor and a 100K_XR resistor.
 - A similar resistor network is connected to the VREF_N input.
- Comparators:** Four comparators (C350, C351, C352, C353) are shown, each with a 100K_XR resistor on its non-inverting input and a 100K_F resistor on its inverting input.
- Outputs:** The outputs of the comparators are connected to a common ground.

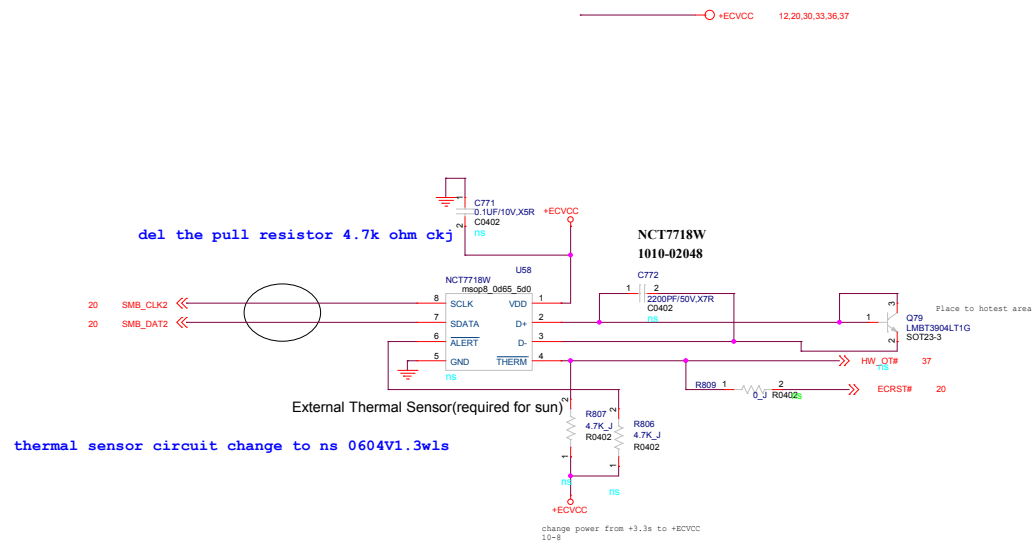
Bottom Diagram: VREF_CAL Block

- Inputs:**
 - VREF_P:** Connected to the non-inverting inputs of comparators C358 and C359.
 - VREF_N:** Connected to the inverting inputs of comparators C358 and C359.
- Resistor Network:**
 - A resistor network is connected to the VREF_P input, consisting of a 47K_F resistor in series with a parallel combination of a 100K_F resistor and a 100K_XR resistor.
 - A similar resistor network is connected to the VREF_N input.
- Comparators:** Two comparators (C358, C359) are shown, each with a 100K_XR resistor on its non-inverting input and a 100K_F resistor on its inverting input.
- Outputs:** The outputs of the comparators are connected to a common ground.

FOR EMI 0122

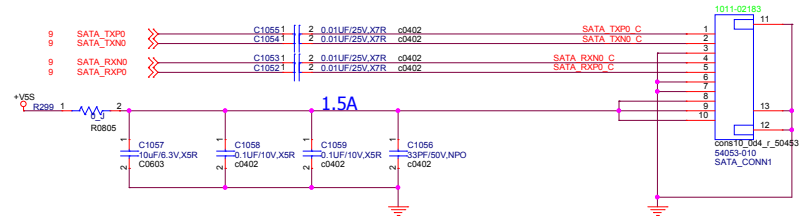


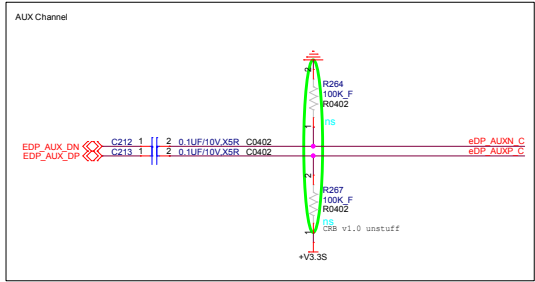




+VSS 25.28,44

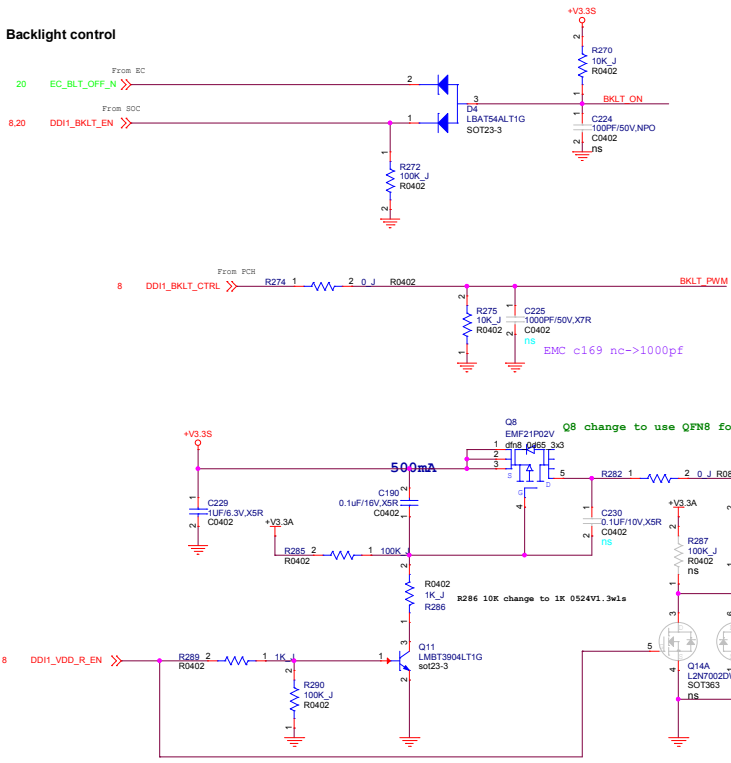
Add CHK2 CHK5 R23 R19 R31 R29 FOR EMC 0415



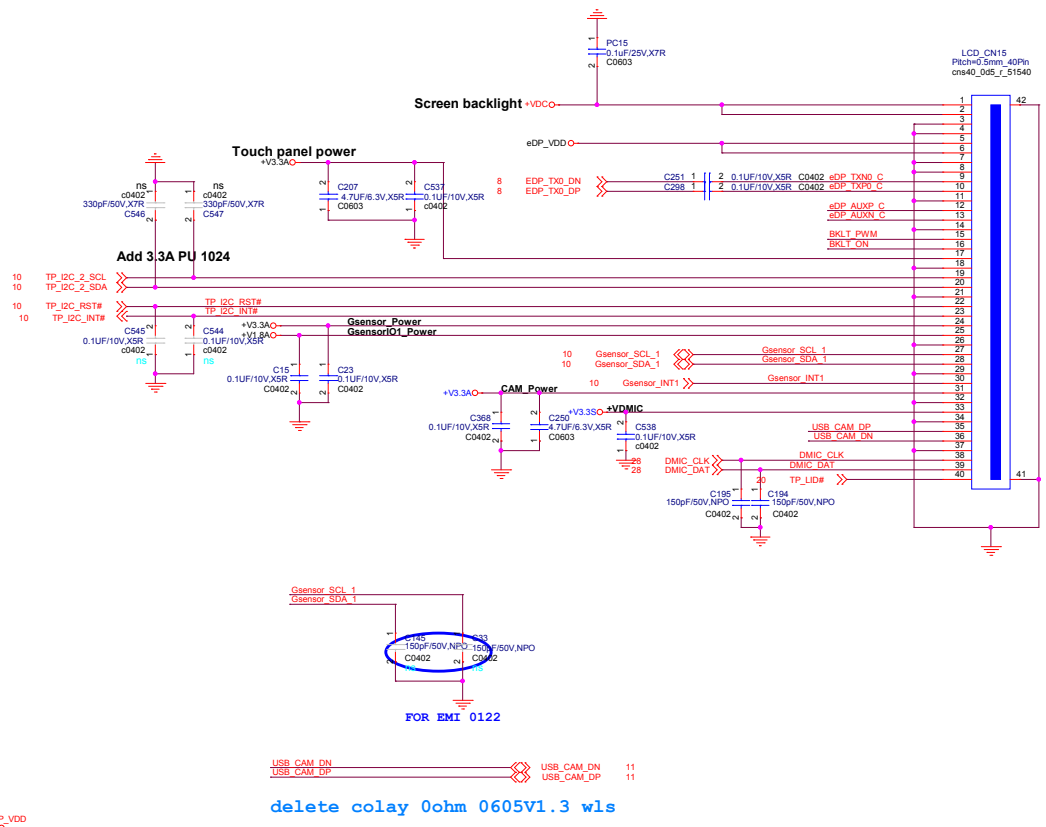


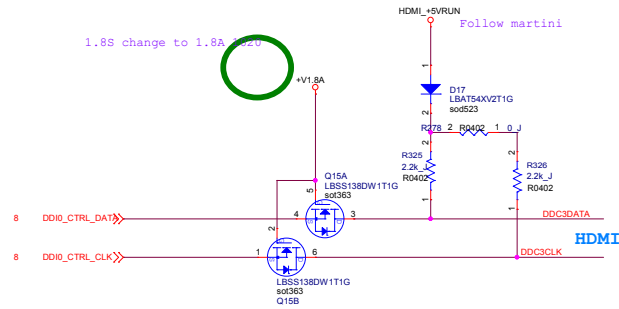
LVDS_CLK-
LVDS_CLK+
LVDS_DATA0-
LVDS_DATA0+
LVDS_DATA1-
LVDS_DATA1+
LVDS_DATA2-
LVDS_DATA2+

Backlight control

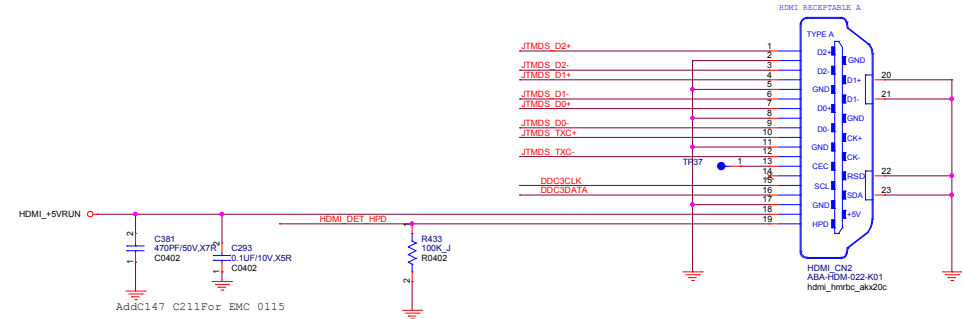
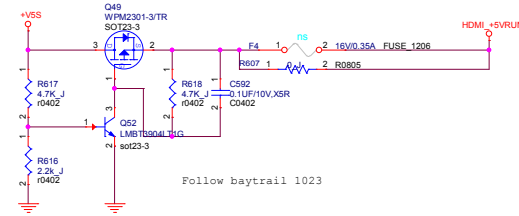
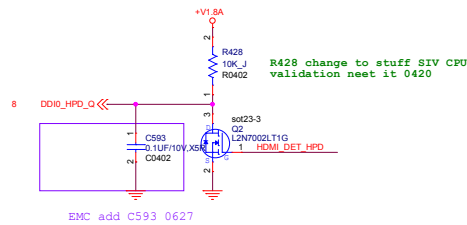
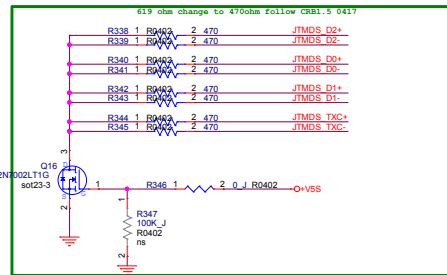


+VDC	36, 38, 40, 42, 44
+V3.3S	7, 8, 14, 20, 23, 26, 28, 31, 32, 34, 44
+V3.3A	7, 10, 12, 20, 26, 28, 33, 34, 37, 44
+V1.8A	7, 12, 14, 16, 20, 23, 26, 27, 31, 36, 44
+V1.8S	10, 14, 20, 23, 28, 31, 44

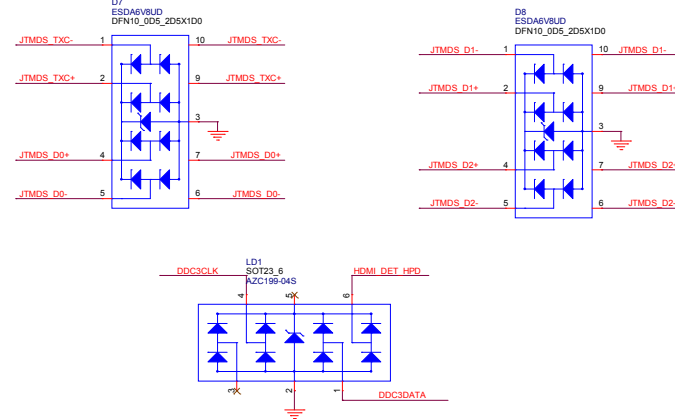


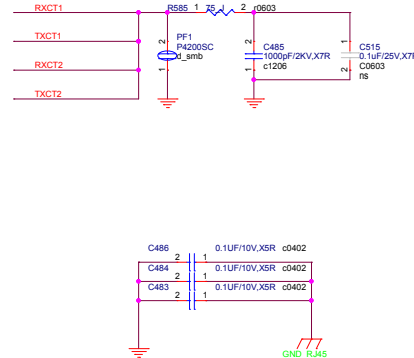
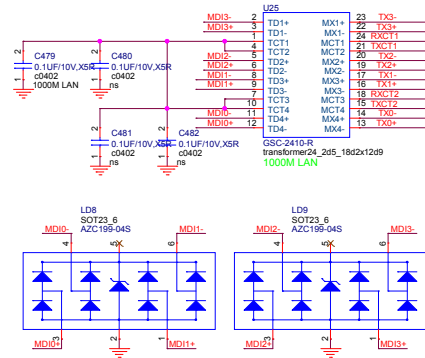
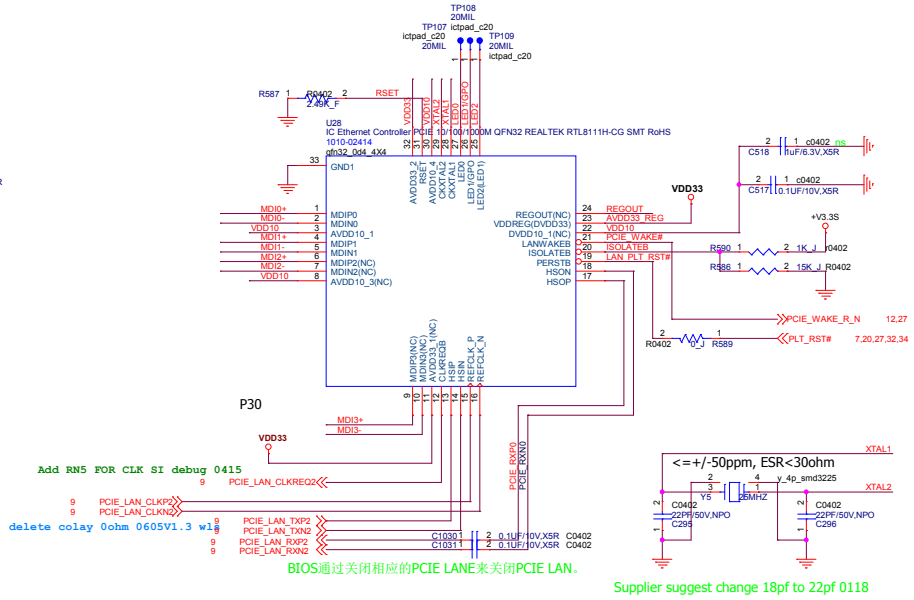
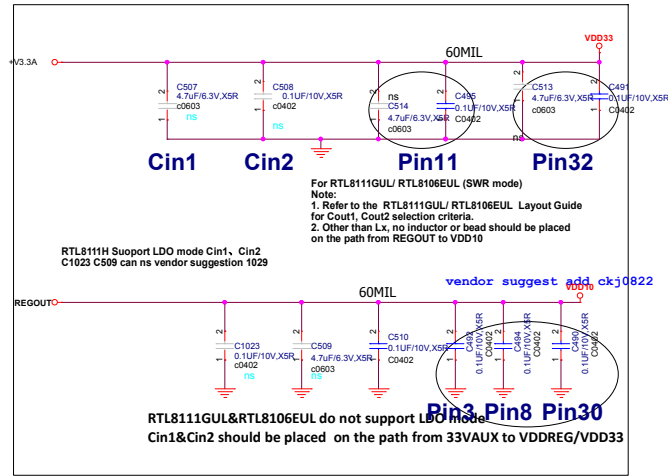


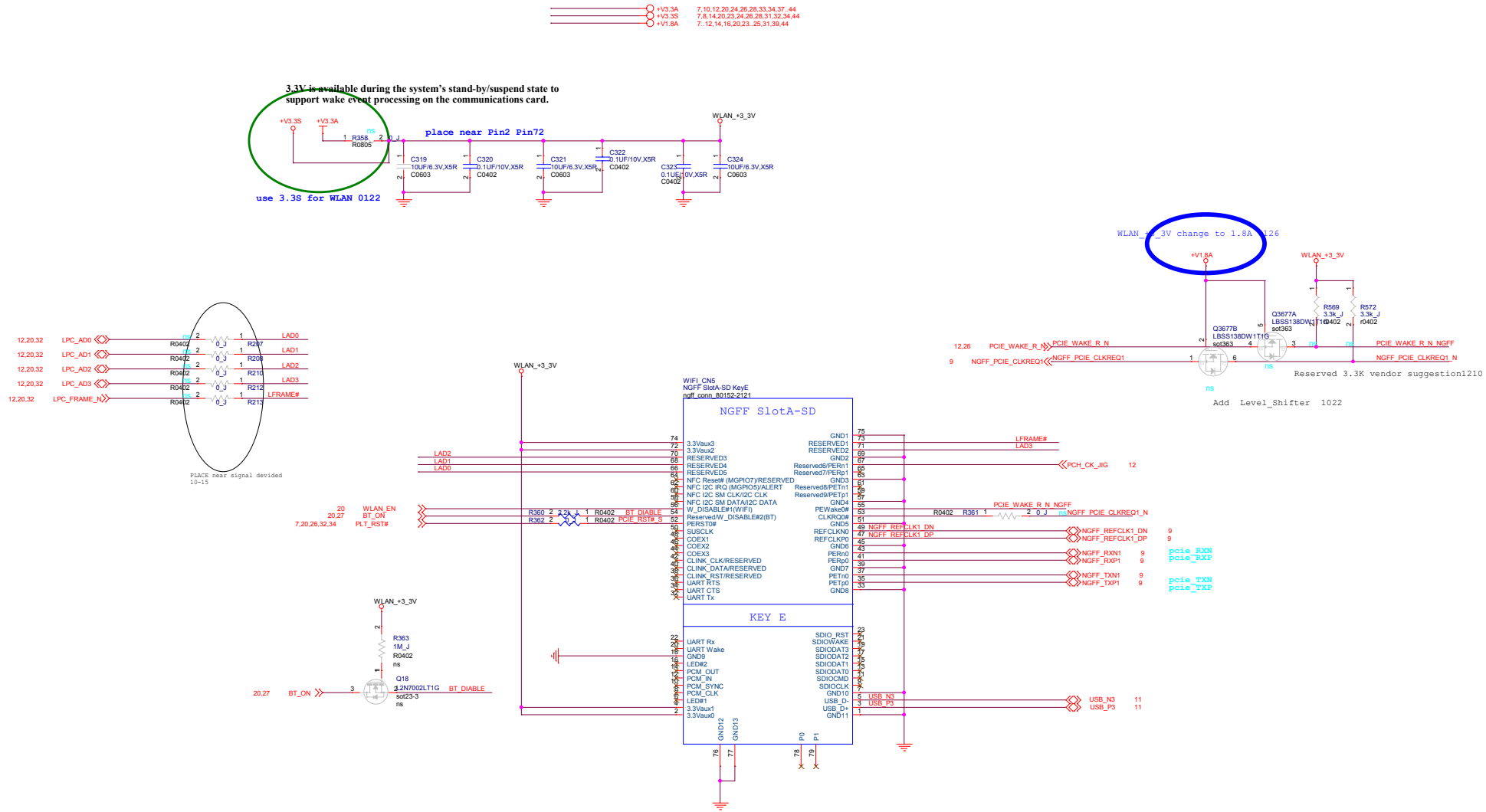
delete colay 0ohm 0605V1.3 wls

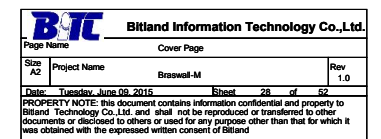


HDMI

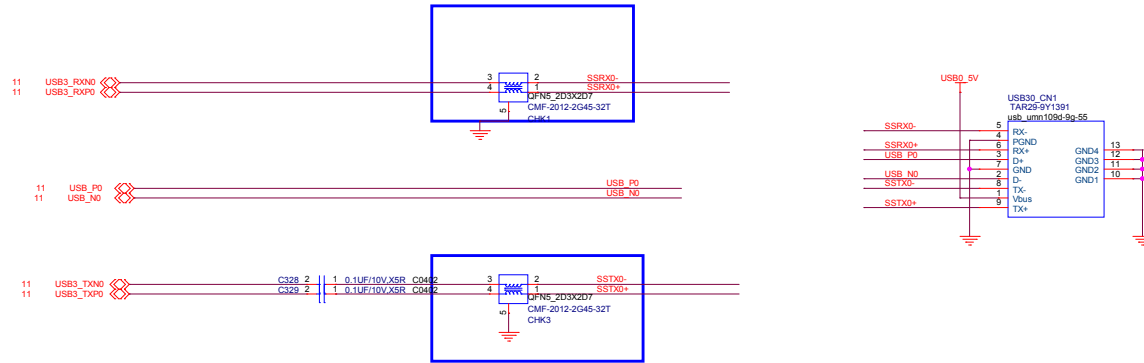




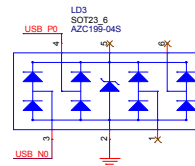
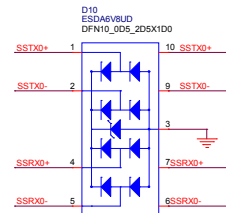
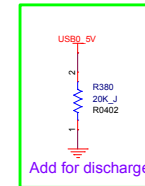
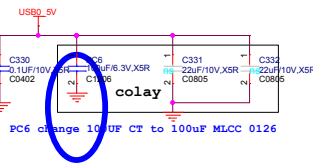
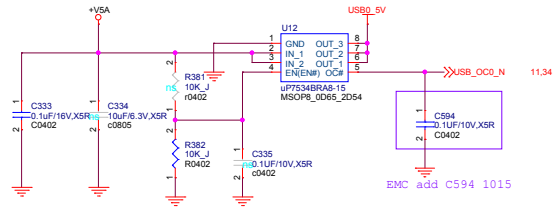


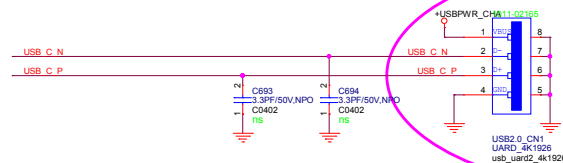
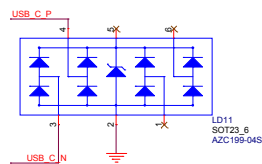


chk1 chk3 FOR EMI SIV 0122

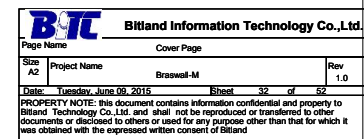


Intel recommends each USB3.0 slot be capable of supplying a minimum of 0.9 A



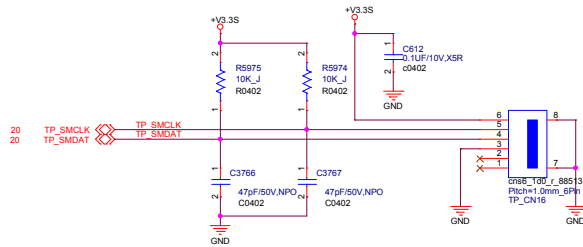


USB2.0 port





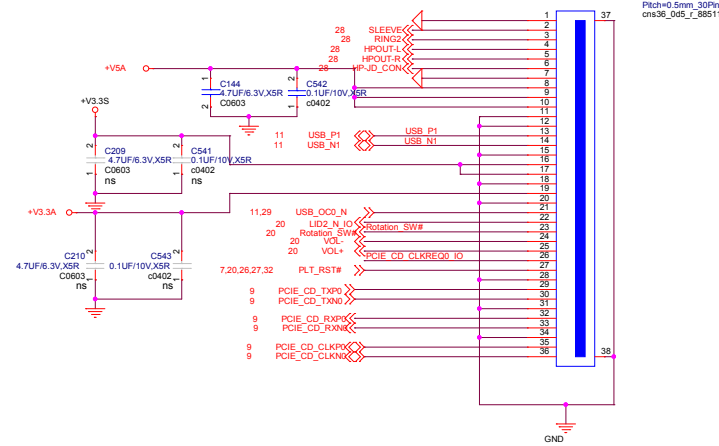
Tocuh pad



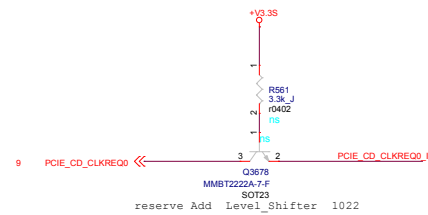
BM连接BH PIN顺序TBD

J1 Pin Assignments and Definitions

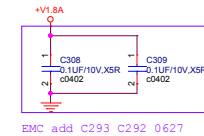
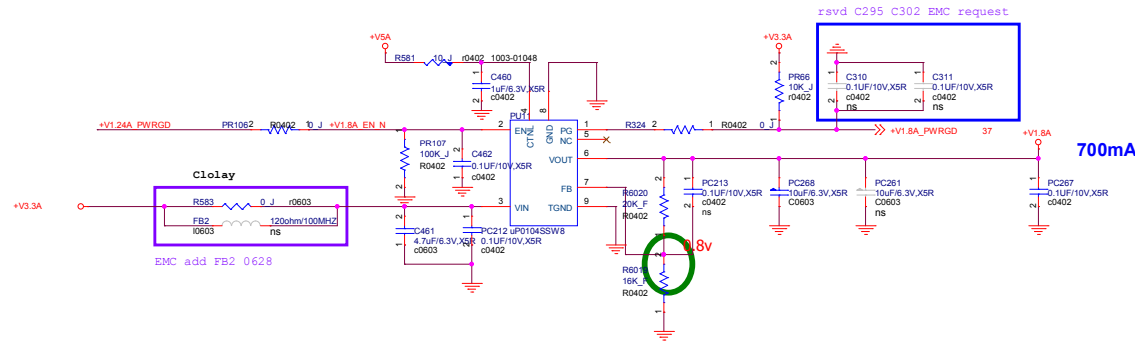
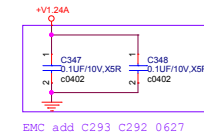
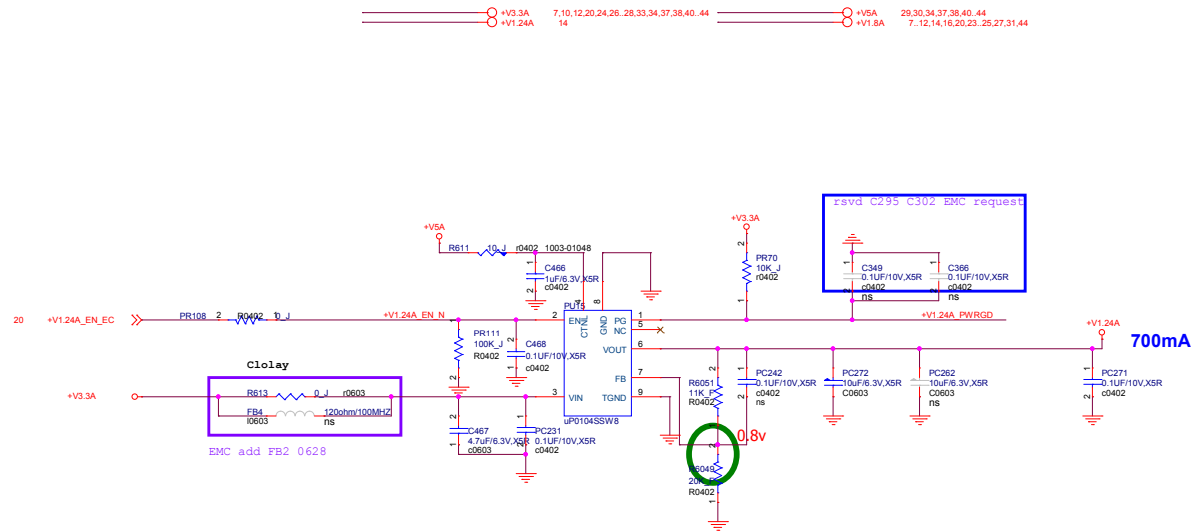
Pin Number	Pin Name	Description
1	VDD	Power Supply Voltage
2	PS2_CLK	PS/2 Clock
3	PS2_DATA	PS/2 Data
4	GND	Ground
5	SMBCLK	SMBus + Clock
6	SMBDAT	SMBus + Data

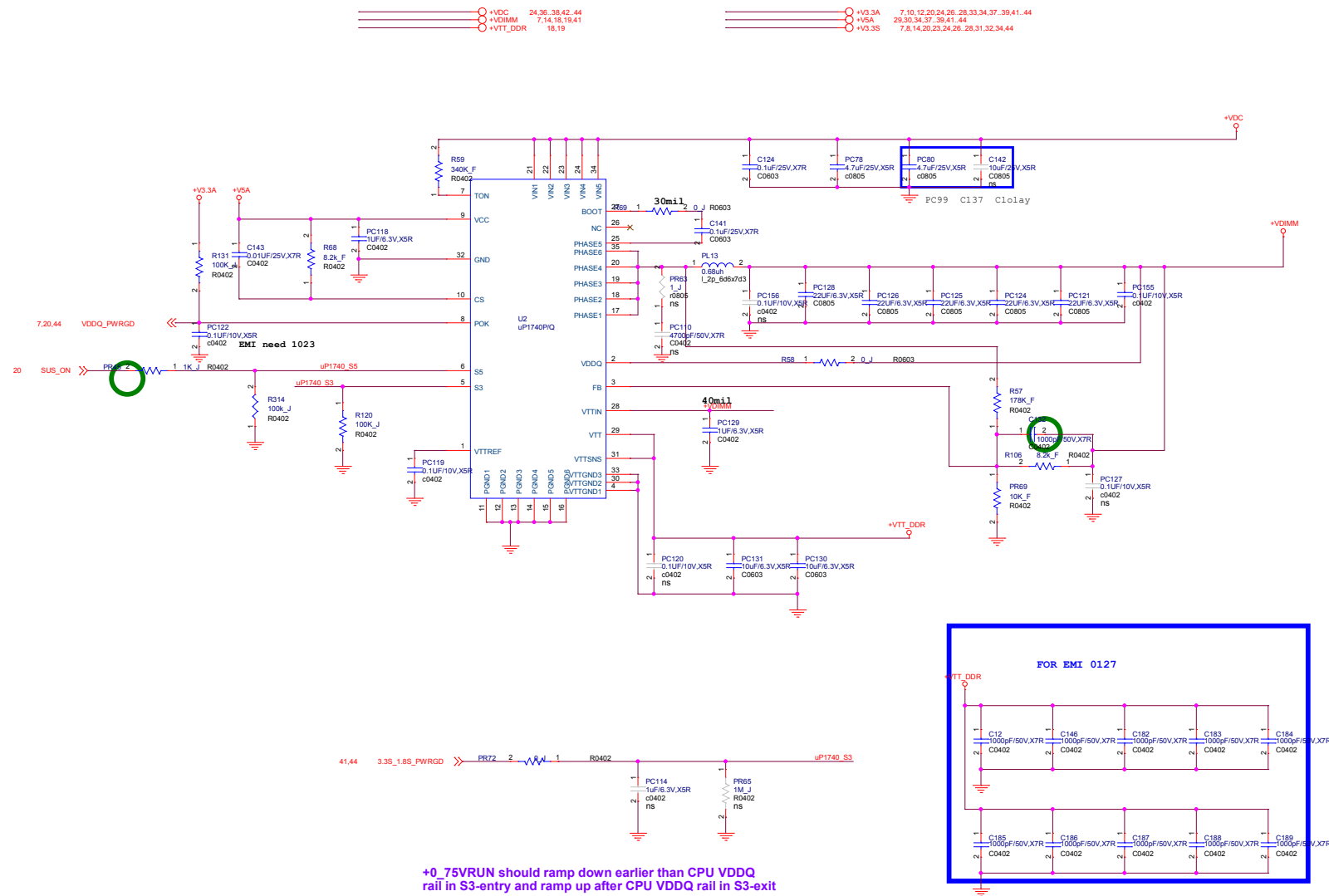


reserve LID2 to SOC



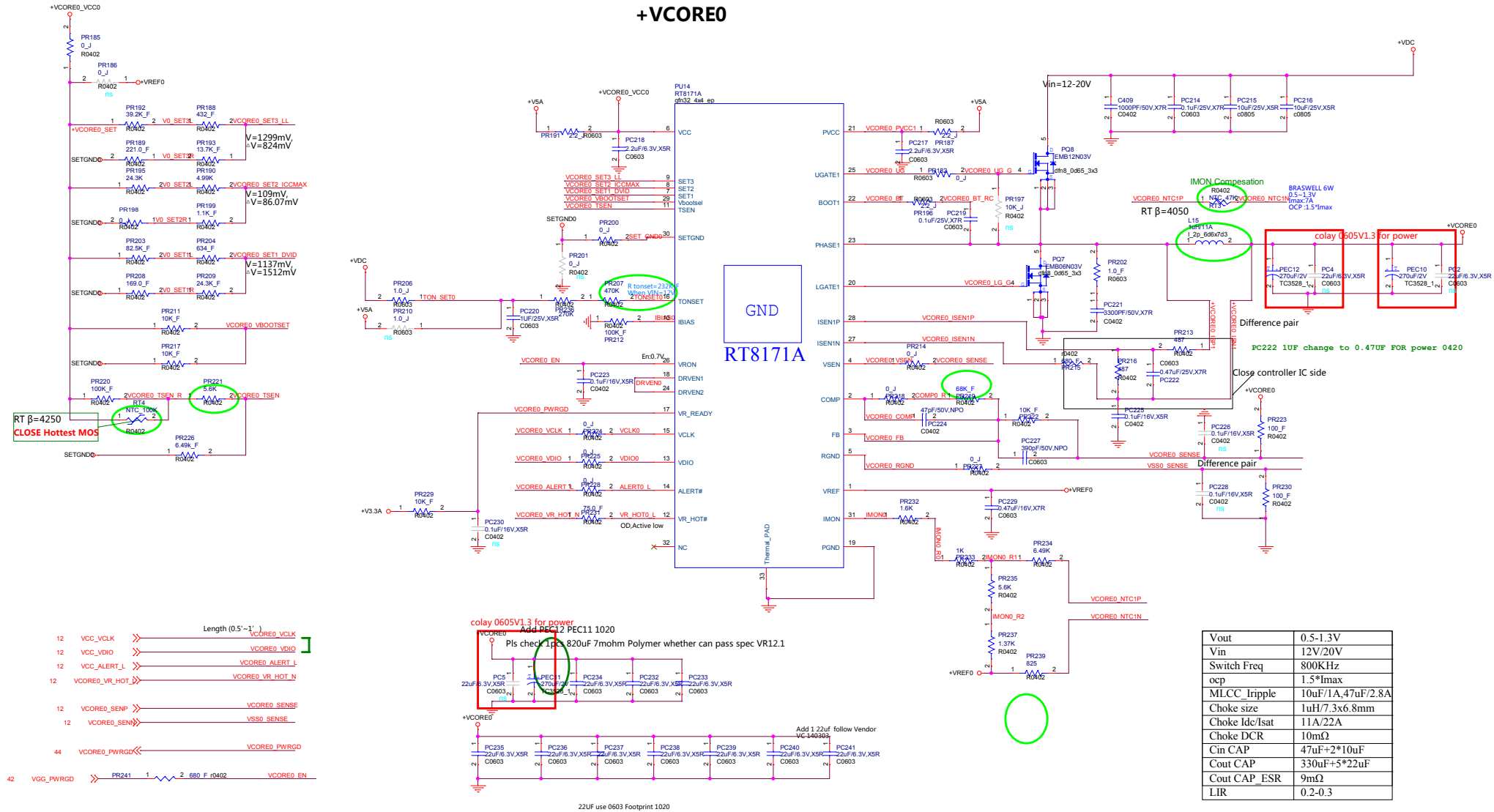
reserve Add Level_Shifter 1022

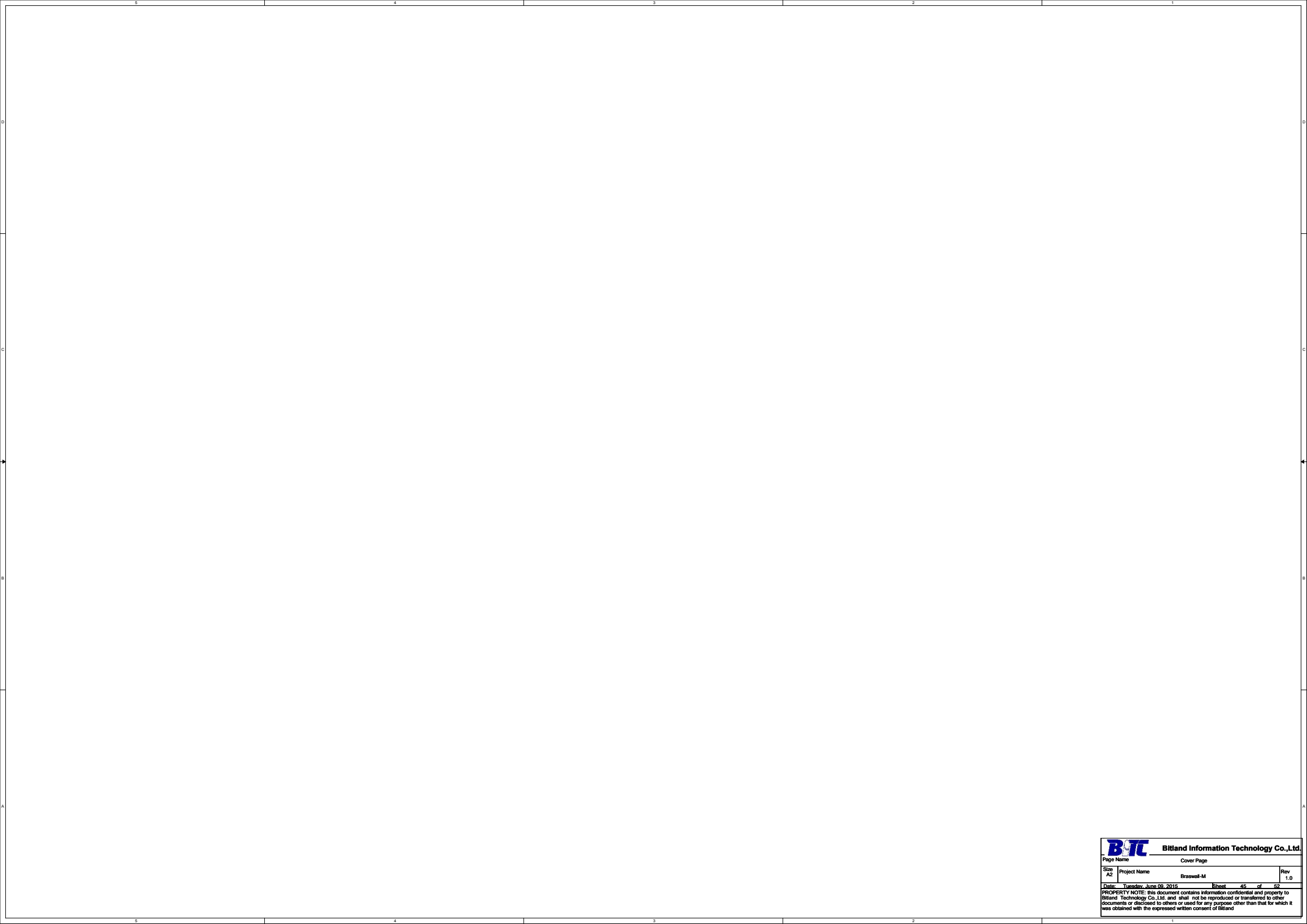


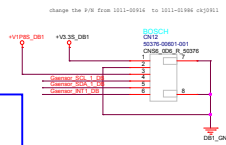


+VCORE0

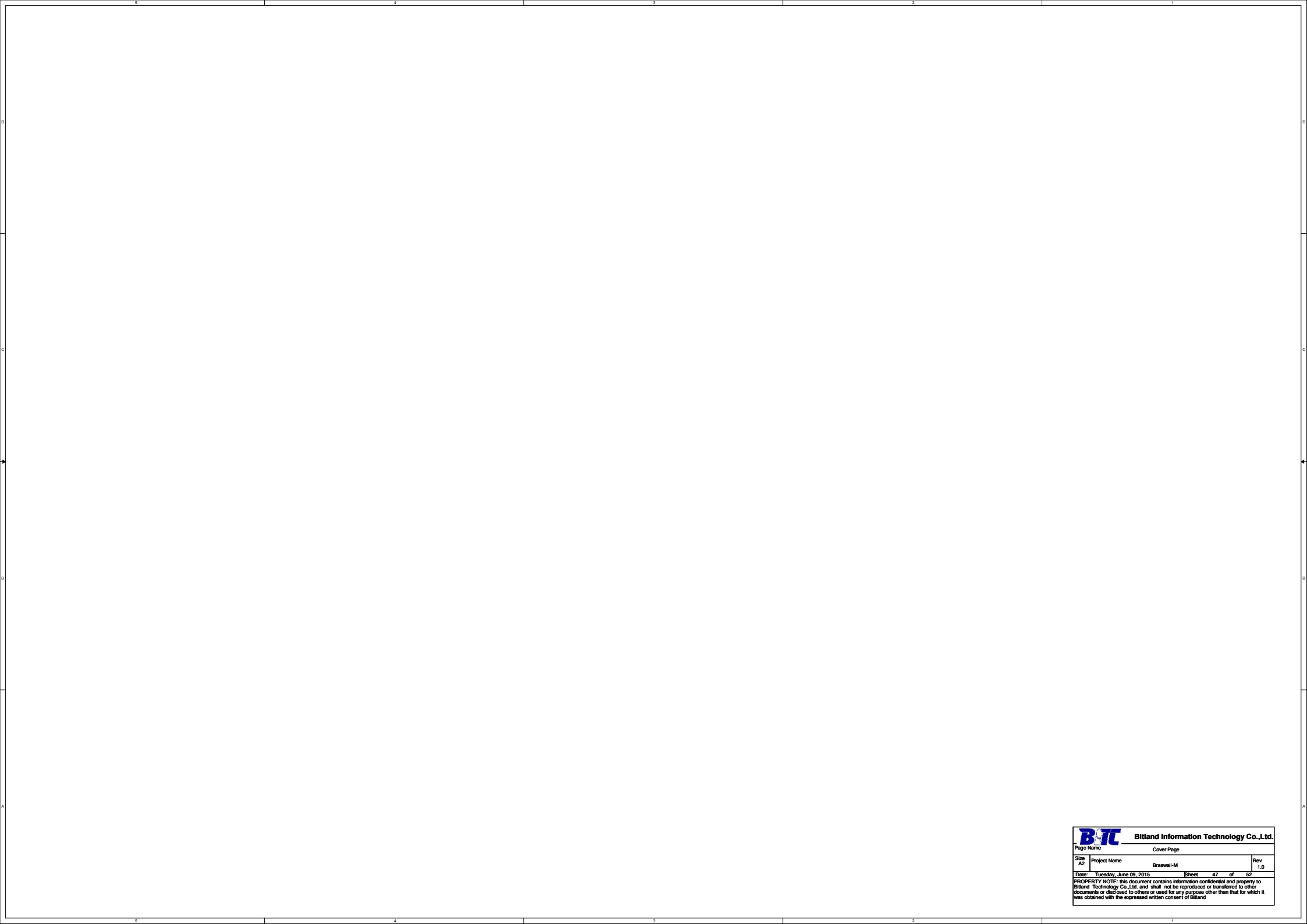
+VCORE0	13	+V1.05A	12, 14, 38
+VDC	24, 36, 38, 40, 42, 44	+V3.3A	7, 10, 12, 20, 24, 26, 28, 33, 34, 37, 42, 44
+V5A	29, 30, 34, 37, 42, 44		

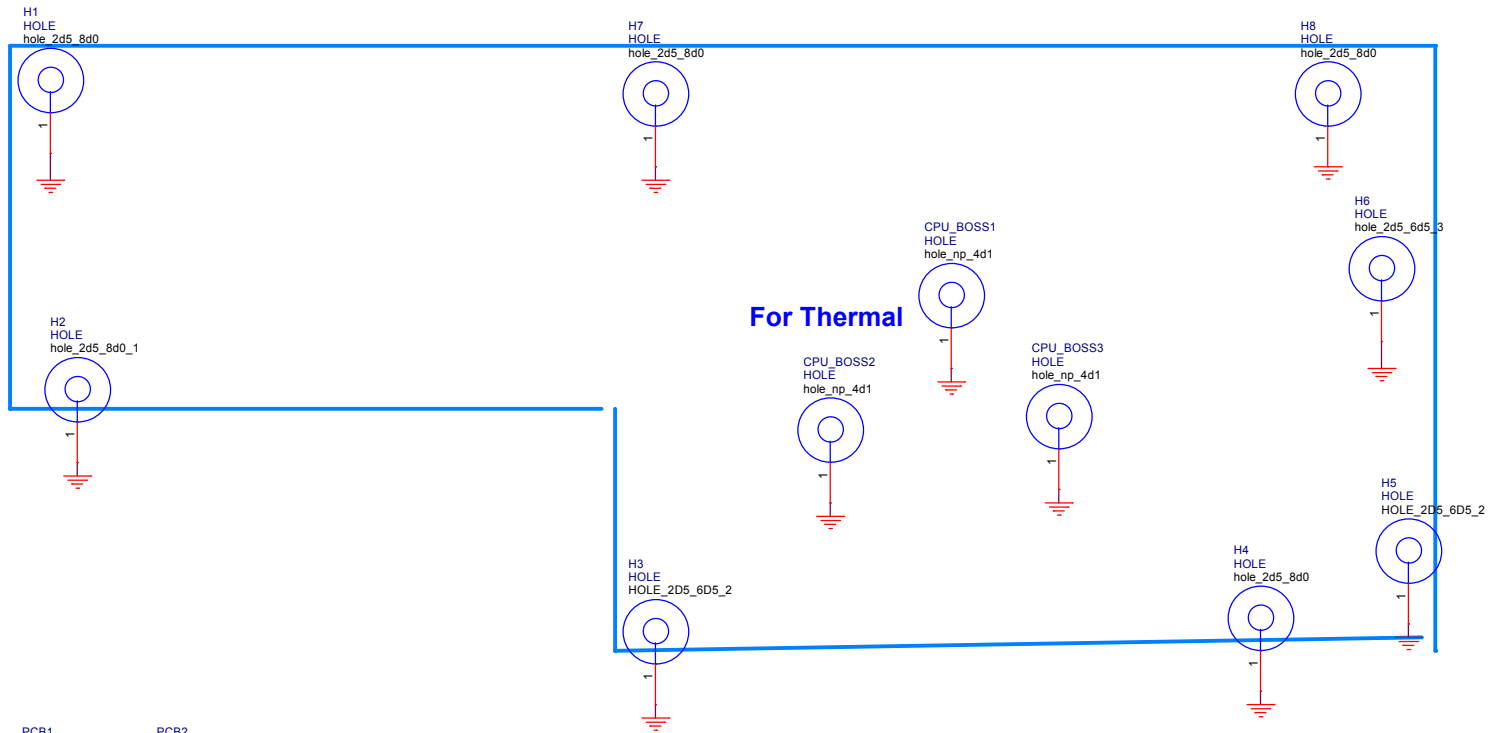


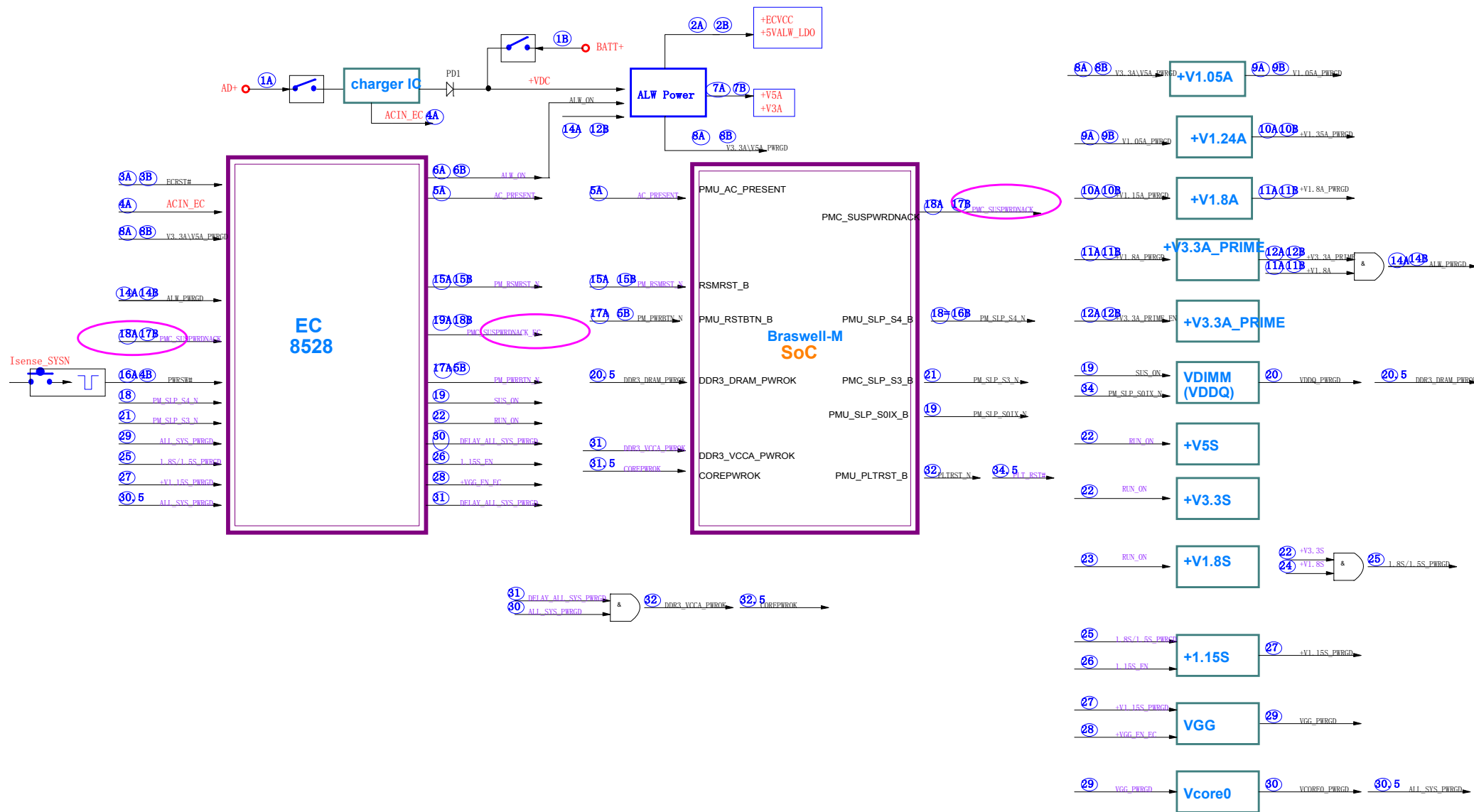


[illegible]

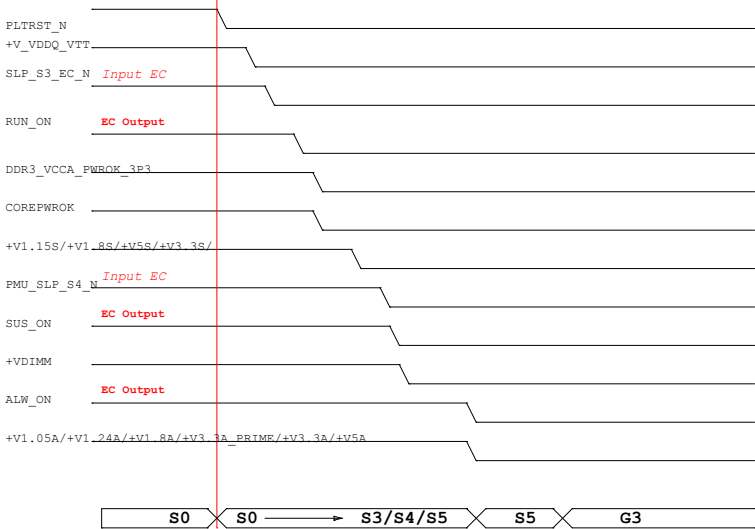
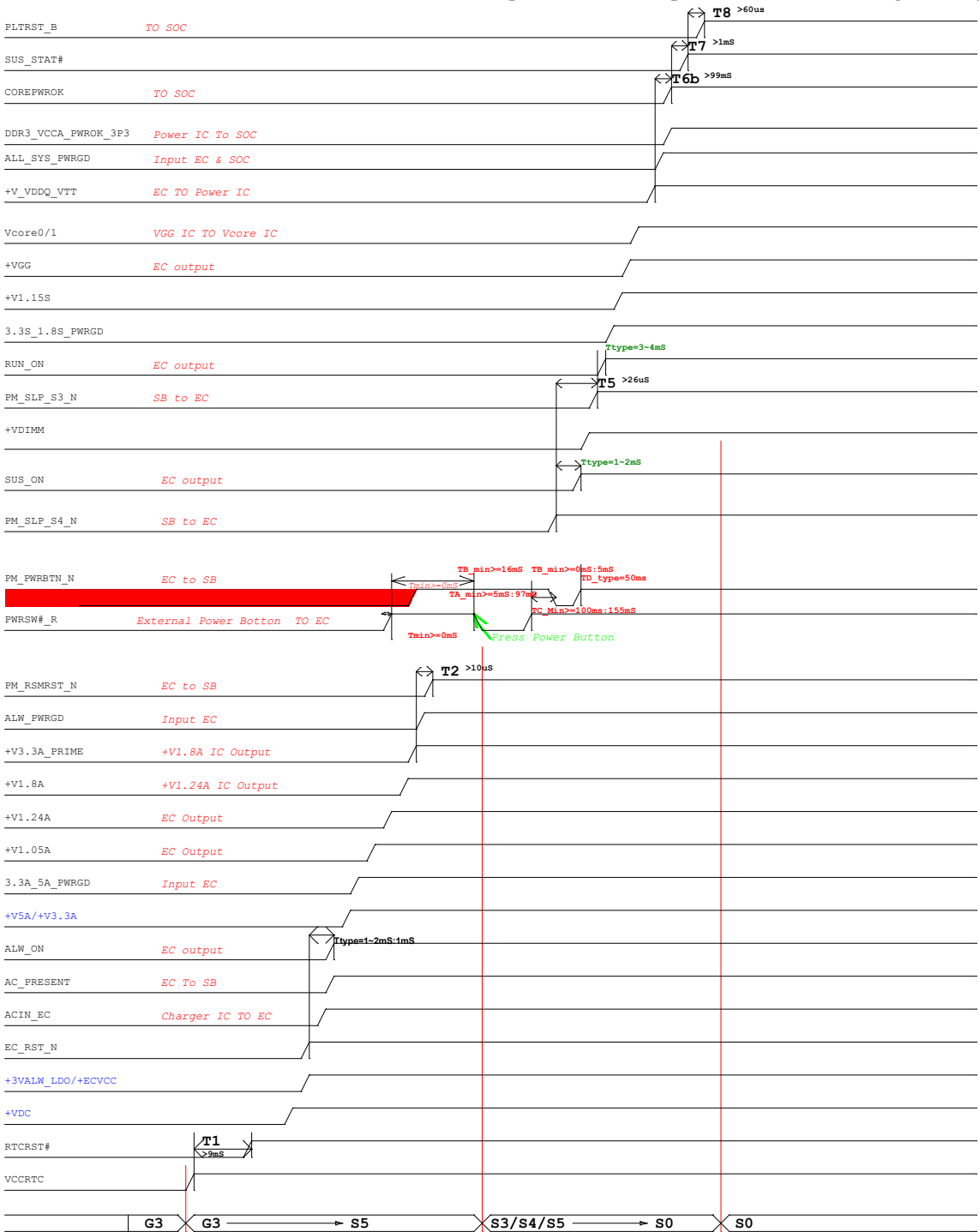
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Size A1	Project Name Brennwald	Rev 1.0	
Date: Tuesday, Aug 09, 2011 10:58 AM			
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Power On/Off Sequence Specification(Adapter Mode) G3-S5-S4-S3-S0



条纹填充区域表示在这段时间任意一个时间点达到要求电平都OK


Power On/Off Sequence Specification(Battery Mode) G3-S5-S4-S3-S0



条纹填充区域表示在这段时间任意一个时间点达到要求电平都OK

Change History

Version	Notes	Date
V1.0	Initial release	2014.10.11
V1.1	SIV	
V1.2	SIT	
V1.3	SVT	



Bitland Information Technology Co.,Ltd.

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